

FIG. 7



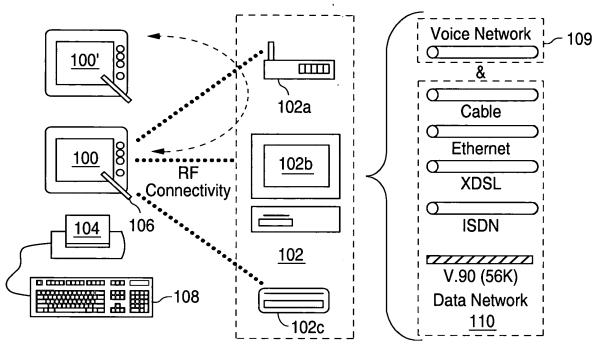


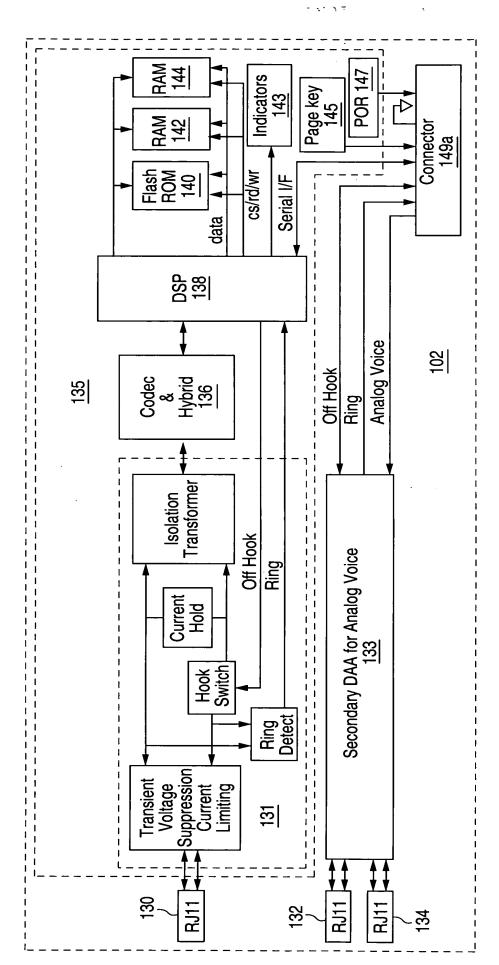
FIG. 2

9550 7

**Processor** DRAM 100 112 114 113 **PCI** Bus **Touch Control** Display 101 Chipset 120 <u>116</u> Microcontroller 127 Codec 118 -117 115 ISA Bus Battery & Charger 129 **123** Flash ROM Transceiver Module 111 125

FIG. 3





**FIG. 4** 

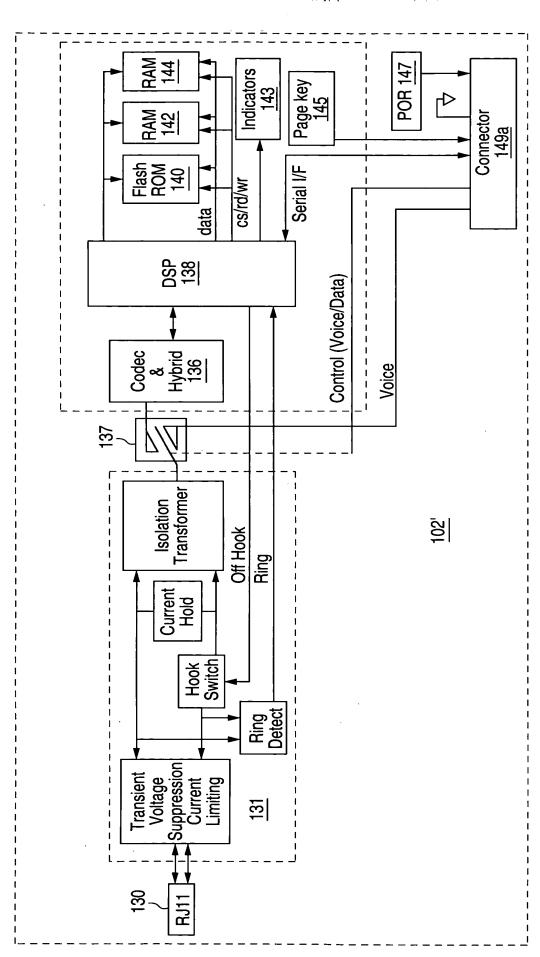


FIG. 5



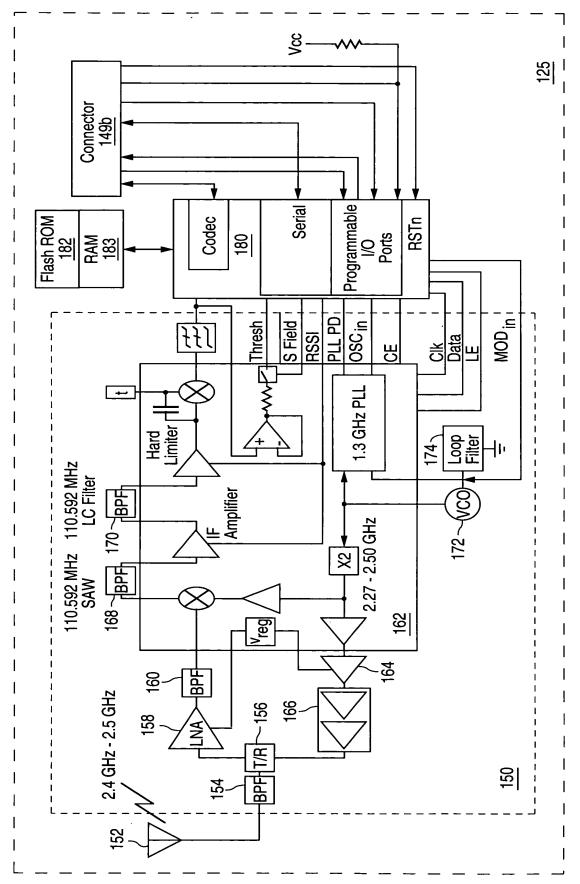
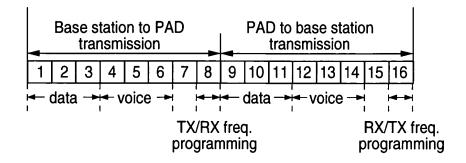
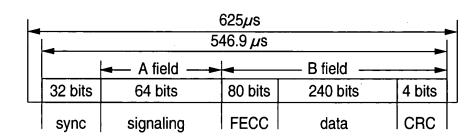


FIG. 6







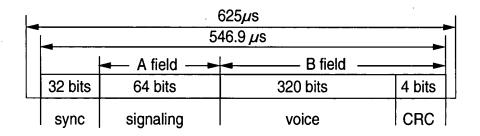


FIG. 8

PREAMBLE		HEADER			DATA
SYNC WORD 80 BITS	FRAME TIMING 16 BITS	DATA WORD LENGTH 12 BITS	DATA RATE 4 BITS	ERROR CHECK WORD 16 BITS	DATA 1-4095 BYTES
128 BITS —					

FIG. 9 (PRIOR ART)